REMARKS

Claims 1 and 3-8 are pending in this application. In this Amendment, claim 1 has been amended. Care has been exercised to avoid the introduction of new matter. Support for the amendment of claim 1 can be found in, for example, Fig. 5 and relevant description of the specification.

Information Disclosure Statement

The Office Action dated May 3, 2006, has acknowledged the submission of the Information Disclosure Statement of April 12, 2004, and stated that the cited references have been considered. It is noted, however, that the form PTO-1449 exhibits the Examiner's initials for only two of the three references that were submitted and listed on the form, presumably an inadvertent error. **Acknowledgement of consideration of the AMBA publication in a further copy of the PTO-1449 is respectfully solicited for clarification of the record**.

Claims 1 and 3-8 have been rejected under 35 U.S.C. §102(b) as being anticipated by Ganapathy et al.

In the statement of the rejection, the Examiner asserted that Ganapathy et al. discloses an apparatus for distributed direct memory access for systems on chip identically corresponding to what is claimed.

Applicant submits that Ganapathy et al. does not disclose a direct memory access controller including all the limitations recited in independent claim 1. Specifically, the reference does not disclose, at a minimum, "said direct memory access controller further comprises a cycle steal control circuit receiving a control signal from an arbiter to control the control portion such

that bus ownership is passed to another channel in a prescribed order and the bus ownership is passed among channels at every prescribed number of transfers," recited in claim 1.

Ganapathy et al. discloses, "[a] round-robin arbitration scheme on the system bus 200 assures that each of the distributed DMA master controllers 203A-203N, 207 and 215 have access every so often to the system bus 200 and can access the global memory 210 at that time," (paragraph [0019]). However, Ganapathy et al. merely discloses that when a DMA transfer of one DMA master controller is ended, bus ownership is passed to another DMA master controller. In contrast, the claimed cycle steal control circuit is configured for controlling the control portion such that bus ownership is passed to another channel in a prescribed order and the bus ownership is passed among channels at every prescribed number of transfers. Ganapathy et al. is silent on this limitation of claim 1.

Based on the foregoing, Ganapathy et al. does not identically disclose a direct memory access controller including all the limitations recited in independent claim 1 within the meaning of 35 U.S.C. §102. Dependent claims 3-8 are also patentably distinguishable over Ganapathy et al. at least because these claims respectively include all the limitations recited in independent claim 1. Applicant, therefore, respectfully solicits withdrawal of the rejection of claims 1 and 3-8, and favorable consideration thereof.

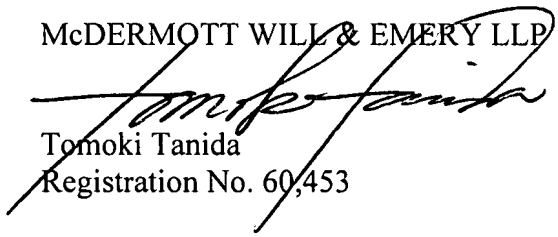
Conclusion

It should, therefore, be apparent that the imposed rejections have been overcome and that all pending claims are in condition for immediate allowance. Favorable consideration is, therefore, respectfully solicited.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

McDERMOTT WILL & EMERY LLP



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